UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,878	02/25/2004	Jeffrey Raynor	02ED143352632	1909

27975 7590 12/22/2006

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
LOUIE, WAI SING	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,878	RAYNOR, JEFFREY	
	Examiner	Art Unit	
	Wai-Sing Louie	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,12,14,15,17,19-21,24-26 and 36-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12,14,15,17,19-21,24-26 and 36-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-16, 19, 23, 26, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (US 6,569,700) in view of Rhodes (US 6,723,594).

With regard to claims 11, 17, 20, 24, 38, and 42, Yang discloses a photodiode device (col. 2, line 43 et seq. and fig. 2) comprising:

- A photodiode 60 comprising:
    - A well 50 of second conductive type (n-type) having opposing sides and positioned in the layer 44, the well 50 defining a photodiode collection node 46 (col. 2, lines 43-50 and fig. 2);
    - An isolation trench 58 partially bounding an upper portion of the n-well 50 at the opposing sides and comprising a shallow trench isolation (STI) having a depth from the upper surface of the layer less than the depth of the well (col. 2, lines 43-50 and fig. 2);
    - Yang does not disclose an epitaxial layer of a first conductive type (p-type) and having an upper surface. However, Rhodes discloses an epitaxial

layer 20 of a first conductive type formed on the substrate 16 (Rhodes col. 7, lines 5-13 and fig. 5). Rhodes teaches the epitaxial layer is utilized to form regions/junctions in the base semiconductor structure (Rhodes col. 3, lines 15-22) and the CMOS imager device has a low power consumption (Rhodes col. 1, lines 58-66). Therefore, it would have been obvious to one of ordinary skill in the art to modify Yang's device with the teaching of Rhodes to form an epitaxial layer on top of the substrate in order to form regions/junctions in the base semiconductor structure and have a low power consumption device.

With regard to claims 12, 21, and 39, Yang discloses the STI completely bounds the upper portion of the well (fig. 2).

With regard to claims 14 and 40, Yang discloses the well 50 comprises an n-well (col. 3, line 41).

With regard to claims 15 and 41, Yang modified by Rhodes disclose an epitaxial layer 18 having a p-well 20 formed in layer 16 (Rhodes col. 3, lines 1-10).

With regard to claim 25, Yang discloses a pn junction is formed at the interface between the STI 52 and the well 50 (fig. 2).

With regard to claim 19, 26 and 36, Yang modified by Rhodes do not disclose the width of the photodiode is less than or equal to 10 micrometers and the depth of the STI is 2-3 micrometers. The width and depth are considered to involve routine optimization, which has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection

of reaction parameters such as temperature, thickness, depth, and width etc. would have been obvious:

> "Normally, it is to be expected that a change in temperature, or in thickness, or in time, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any width and depth suitable to the method of the process in order to optimize the design.

With regard to claim 37, in addition to the limitations disclosed in claims 11 and 20 above, Yang modified by Rhodes also disclose:

- The isolation trench having a width substantially extending over the width of the pixel (fig. 2);
- A pn junction being formed at an interface between the STI and the well (fig. 2).

Response to Arguments

Applicant's arguments filed 9/12/2006 have been fully considered but they are not persuasive.

- Applicant argues that Yang teaches away from the recited epitaxial layer by disclosing polycrystalline layers (col. 2, line 51 to col. 3, line 23). However, the polysilicon layer 66 is in the intermediate process (it is removed from the final product). The final product in fig. 2 does not disclose not contain a polysilicon layer (col. 2, line 8). Rhodes discloses an epitaxial layer, where the epitaxial layer facilitates to form device and junction in the layer. Rhodes provides a motivation to combine, which is the CMOS imager device formed in the layer have a low power consumption. Therefore, the combination of Yang and Rhodes is proper.
- Applicant argues the new claims 37-42 claims the STI and the n-well having a width substantially extending over the width of the pixel. However, Yang discloses the STI surrounding the photodiode region and other units to reduce the leakage current (col. 2, lines 1-19) and Rhodes discloses the STI's 112 are formed around the pixel cell 14 (Rhodes col. 8, lines 43-57 and fig. 7). Therefore, Yang and Rhodes both disclose the STI and the photodiode region (n-well) substantially extending over the width of the pixel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (571) 272-1709. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WAI-SING LOUIE
PRIMARY PATENT EXAMINER

Wsl
December 15, 2006.